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LDRD PROJECT NUMBER: 188026
LDRD PROJECT TITLE: Vertical GaN PIN diodes with 5 kV avalanche breakdown
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ABSTRACT:

High voltage diodes are desired for many high power switching applications. GaN pin diodes have the potential to replace conventional silicon diodes for applications requiring very low size and weight, and high power. GaN diodes have several advantages including the ability to operate at high temperatures and a higher tolerance to radiation damage. The focus of this exploratory express LDRD is to develop a detailed understanding of GaN pin diodes with the goal of demonstrating devices with a reverse breakdown voltage of greater than 5 kV. Although the breakdown voltage is nominally determined by the thickness and doping of the drift region, it is known that the edge termination of the device is of critical importance in achieving the optimum reverse bias characteristics. Therefore, as a part of this project, edge termination effects were carefully investigated both experimentally and theoretically in order to understand GaN pin device operation. Specifically, we investigated the impact of the thickness of the implanted region in the p-type GaN layer and its effect on reverse bias characteristics. Through proper design and fabrication of GaN pin diodes it is possible to demonstrate devices with a 5 kV or greater reverse bias breakdown voltage.

INTRODUCTION:

Although wide band gap electronics have the potential to revolutionize electrical power conversion, much work remains to make this vision a reality. Wide band gap devices made from SiC and GaN are already performing better that their Si counterparts with respect to high voltage operation. One of the primary reasons for this is that wide band gap materials have a very high critical field for electrical breakdown. In fact, the wider the band gap of the semiconductor material, the higher the critical field. This means that it is possible to hold off very high reverse bias voltages using a single GaN pin diode operating in reverse bias. Other factors such as high temperature operation and radiation hardness also make GaN devices very attractive for many applications.

While we originally proposed to carefully examine the fundamental critical field for GaN, in the end, we focused on edge termination effects as this was the effect that was limiting the device performance. We decided that a detailed understanding of certain aspects of edge termination would allow us to understand GaN pin devices at a deeper level and make rapid improvements in device performance. The knowledge gained here on edge termination effects will pay dividends in advanced device performance for many future generations of GaN pin devices. Although a careful experimental determination of the critical field would also be very beneficial, that work was not performed as a part of this project and will be a subject for future research.

Many designs for edge termination include very complicated structures where as many as 14 rings of various widths are fabricated. The rings are implanted with nitrogen or hydrogen to deaden the p-type material in each ring. The intent of these ring structures is to spread out the

electric field at the edge of the junction such that there is no one spatial region with a very high electric field. The device will break down under reverse bias wherever the electric field is the highest, which is usually at the edge of an abrupt junction termination. Based on these arguments, some sort of edge termination is almost always used to increase the reverse bias breakdown for high voltage GaN pin devices.

During our initial design, fabrication, and testing of GaN pin devices for high voltage operation, we found that devices with 14 rings often had a poor reverse bias breakdown voltage and devices that had no rings often had very high breakdown voltages. This is a very interesting and potentially useful result as it shows that very high voltage devices can be realized without needing to design and fabricate complicated ring structures. This result is very counterintuitive and required further investigations. Thus, a major part of the work on this LDRD was focused on gaining a detailed experimental and theoretical understanding of how p-GaN thickness and implant depth impact the reverse bias breakdown voltage. Our working theory is that if the depth of the implant and the p-GaN thickness are adequately controlled, a simple edge termination scheme can be used to maximize the reverse bias breakdown voltage without the need for a complicated ring structure.

DETAILED DESCRIPTION OF EXPERIMENT/METHOD:

For this work, the GaN pin devices studied were grown on bulk GaN substrates. The use of bulk GaN substrates is critical to the high voltage performance for GaN diodes. InGaN LEDs are primarily grown on sapphire substrates and have very high internal quantum efficiencies and very long lifetimes between 50,000 and 100,000 hours. However, most InGaN laser diodes are grown on bulk GaN substrates. The main difference between these two device types is the operating current density. Laser diodes are operated at a much higher current density and it has been shown that the device lifetime is low (< 1000 hours) for laser diodes grown on sapphire substrates. Due to the lattice mismatch between sapphire and GaN, growth of GaN on sapphire results in material with a vertical threading dislocation density on the order of 10^8 cm^{-2} or higher. On the other hand, vertical threading dislocation densities of 10^4 - 10^6 cm^{-2} are realized for growth of GaN on a bulk GaN substrate. There is a similar trend for GaN-based diodes. For a GaN diode grown on a sapphire substrate, a diode which is reverse biased beyond breakdown will almost always catastrophically fail resulting in a shorted junction. However, for a GaN diode grown on a GaN substrate, the diode can be reverse-biased beyond breakdown and the diode will controllably avalanche and then can recover once the voltage is reduced. Based on these observations, all of our GaN pin devices were grown on bulk GaN substrates, which is now the common practice for high voltage GaN diodes. The only drawback to growth on bulk GaN substrates is the cost of the substrates. A bulk GaN substrate typically costs about $3000/wafer while a sapphire wafer can cost as little as $50/wafer.

The epitaxial layer structure for the GaN diode is formed by metalorganic chemical vapor deposition (MOCVD) in a Veeco D125 reactor. The growth is performed on 2 inch diameter GaN substrates, grown by hydride vapor phase epitaxy, which are commercially available from Sumitomo Electric Industries. The substrate has an intrinsic electron concentration of $2x10^{18}$ cm^{-3}. The epilayers consist of, first, a 15 μm thick n-type GaN layer doped with Si that has an intrinsic electron concentration of $5x10^{15}$ cm^{-3}. The electron concentration is determined by capacitance-voltage profiling. Next, a 400 nm thick p-GaN layer, doped with a Mg concentration of 2-4 x 10^{19} cm^{-3} is grown. Finally, the structure is topped with a 12.5 nm heavily doped p-GaN

layer to facilitate ohmic contacts. The nominal layer thicknesses are determined at the center of the wafer, but the thickness of the layers can vary up to ~20% over the region where devices were studied. Variations in layer thickness are due to a non-uniform distribution of the group-III alkyl source material.

After growth, the wafer undergoes a fabrication process to create vertical power diodes. A schematic cross section and a scanning electron microscope image of a completed device are shown in Fig. 1. A 150 μm diameter Pd/Au ohmic contact is formed on top of the p-GaN. It is capped with a 154 μm diameter, 1 μm thick Au layer to facilitate wire bonding. The edge termination (ET) structure is formed starting 5 μm outside the edge of the p-contact using three nitrogen implants with different doses and energies to create a flat profile of vacancies. This acts to damage the p-type material and make it insulating down to a desired depth. Individual devices are isolated by creating a 150 nm deep and 5 μm wide ring etched into the p-GaN layer 50 μm from the p-contact. This etch also determines the lateral extent of the ET. The device is covered by a 500 nm thick silicon nitride layer for surface passivation. The n-contact is formed on the bottom of the GaN substrate and consists of a Ti/Al/Ti/Ni/Au metal stack. Electrical testing is then performed to determine the reverse bias breakdown voltage. Voltages as high as 2.7 kV have been measured for devices without any rings.

In order to compare theory and experiment and to gain deeper insight into the edge termination in GaN pin diodes, the reverse bias breakdown voltage was calculated for various geometries (described below). Avalanche breakdown is due to runaway impact ionization which can dramatically increase the current in the device and lead to catastrophic failure if not properly controlled. Impact ionization is the physical process by which free carriers in a region with a high electric field gain enough energy to collide with lattice atoms and create additional electron-hole pairs. Simulations for these processes in GaN pins were performed using Silvaco ATLAS TCAD software. ATLAS uses the Newton iteration method to solve a 2D system of coupled equations including Poisson's equation, electron and hole continuity equations, and carrier generation and recombination equations. Detailed comparison of experiment and simulation allowed us to draw important conclusions regarding edge termination in GaN pin devices.

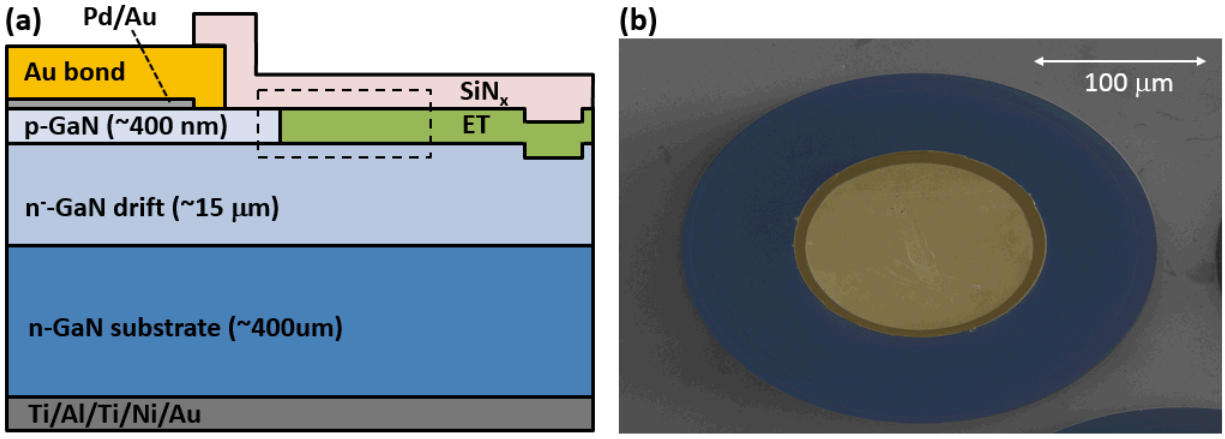

Fig. 1. A (a) cross-sectional schematic and (b) colorized scanning electron microscope image of a vertical GaN power diode. The edge termination (ET) is formed starting 5 μm outside the Pd/Au contact and has a width of ~50 μm. The dashed box in (a) is discussed further below and in Fig. 2.

RESULTS:

As mentioned above, one of the main focusses of this work was to understand why high voltage operation is possible for a sample without any rings in the edge termination scheme. Our basic working theory is that the implanted nitrogen, used to convert p-GaN to insulating GaN, does not completely kill the p-type doping in the p-GaN leaving behind a thin layer of lightly doped p-type material. This thin layer and its thickness appear to be key factors in creating a simple edge termination without the use of a complicated ring geometry. The depth of the implant was modeled using the SRIM software package. This software calculates the number of vacancies as a function of depth. Since the Mg doping level in p-GaN is 2 - 4 x 10^{19} cm^{-3}, we expect to need roughly this density of vacancies to completely compensate the Mg doping and create insulating material. The situation is actually much more complicated and depends on the type of vacancy created and its energy position with respect to the valance and conduction bands. The SRIM software gives the expected profile of vacancies as a function of depth. This vacancy profile varies gradually from approximately 4 x 10^{20} cm^{-3} to zero depending on the ion energy and implant depth into the material. At the level of 4 x 10^{20} cm^{-3}, the material will definitely be insulating. Depending on the thickness of the p-GaN and the depth of the implant, a partially doped p-GaN layer may be present after the implant step.

In order to study this in more detail, we developed a simple model to simulate the impact of a thin lightly p-type doped layer remaining after the implant. Figure 2 shows a schematic of the structure that was modeled using our TCAD software. As an approximation to a graded profile, we modeled our device such that there is a thin layer of p-type material with a hole concentration approximately 10% of the full hole concentration of the unaltered p-type GaN. The existence of this lower doped layer and its thickness are critical in making a simple edge termination without rings. As shown in Fig. 2, the thickness of this layer is labeled t_p. If a thin layer of p-type GaN is grown, the full thickness of the p-GaN will be insulating after implant. For a very thick p-GaN layer as we move deeper into the sample, there be a thick insulting region followed by a graded region, followed by a layer of p-GaN with full conductivity. Both of these situations result in a non-optimal device which has a low voltage reverse breakdown. For a p-GaN layer with an optimum thickness there will be a thin layer (10 – 40 nm) of material with some intermediate level of p-type doping. This is the situation which can lead to high voltage operation for GaN pin diodes. Since the p-GaN thickness varies as a function of position across the wafer, we expect that all three of these conditions can exist on the same wafer.

Figure 3 shows the calculated breakdown voltage as a function of t_p, which is the thickness of

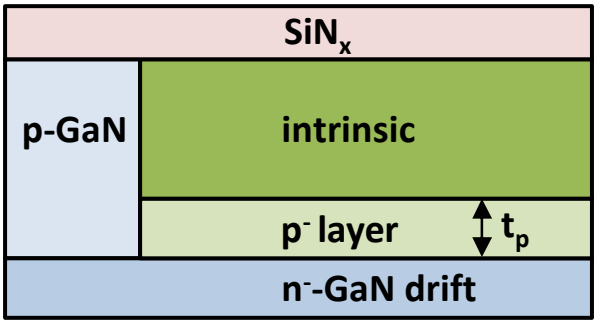

Fig. 2. A cross-sectional schematic of the dashed region in Fig. 1. This shows the simplified geometry for which the TCAD simulation was performed.

the thin layer with lower p-type conductivity. This calculation is performed for the simplified structure shown in Fig. 2. The calculated breakdown voltage shows a peak at about 26 nm with a breakdown voltage of 4.6 kV indicating that there is an optimum thickness for the thin layer t_p. For t_p layers that are too thin or too thick, the breakdown voltage falls off dramatically. Based on these calculations, it is clear that a simple edge termination scheme can be used if the layer thicknesses and implant profile is very carefully controlled. Note that the 4.6 kV calculated breakdown is based on a drift region thickness of 15 microns and carrier concentration in the intrinsic region of 5×10^{15} cm^{-3}. For thicker intrinsic regions and for lower doping levels, higher breakdowns are possible using these same methods. In the next section we will compare these results to breakdown voltages on actual devices and investigate the thickness variation as a function of position across the wafer.

DISCUSSION:

Based on the calculation results shown in the last section, it is clear that the thickness of the p-GaN layer is a very important parameter. This is simply because the implant depth and associated vacancy profile will be fixed by the parameters of the implant and the p-GaN thickness is known to vary across the wafer. In order to investigate this further we measured the breakdown voltage as a function of position across one quarter of a 2 inch wafer. The vertical GaN power diodes are probed and measured on-wafer under DC bias. Reverse-bias measurements are performed in fluorinert to avoid dielectric breakdown in air or at the surface of the device. At large reverse biases these power devices exhibit avalanche breakdown and recover as expected when the voltage is reduced. The breakdown of the various devices varies greatly over the wafer. Breakdown voltages between 400-2600 V were measured and all exhibit avalanche breakdown. This data is shown in Fig. 4. Note that there is a specific region where the breakdown voltage is as high as 2.7 kV. The p-GaN thickness is known to vary as a function of position across the wafer and the best performing devices are probably near the thickest part of the wafer. Therefore, the data shown in Fig.4 are at least qualitatively consistent with the results from TCAD simulations. These experimental results combined with theory give us a reasonable explanation of the achieved voltages for diodes without complicated ring structures and point towards a simple method of achieving high voltages from GaN diodes.

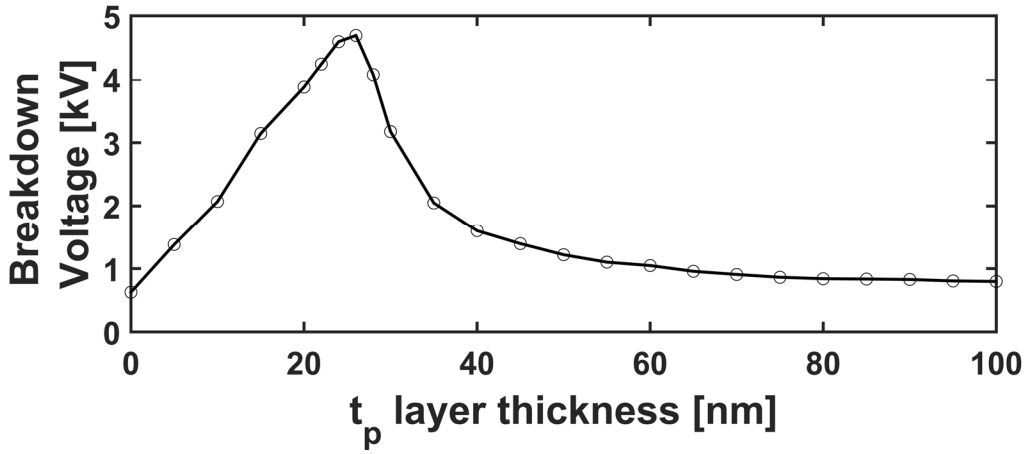

Fig. 3. Calculated breakdown voltage plotted as a function of t_p for the geometry shown in Fig. 2. Note that there is a peak in the breakdown voltage for a layer thickness of approximately 25 nm.

However, it is important to note that many parameters are likely changing as a function of position on the wafer. Thickness variations for different layers are expected to vary by as much as 20% across the wafer where the maximum in thickness occurs at a position that is approximately 20 mm from the flat. Variations in layer thickness are due to a non-uniform distribution of the group-III alkyl source material in the growth reactor. With additional effort and additional growth runs the uniformity across the wafer could be improved. However, the variation across the wafer is actually very useful in helping to figure out the dependence of the breakdown voltage on the thickness of the p-GaN layer.

There are also other factors that vary as a function of position on the wafer. The most important of these is related to the carrier concentration in the intrinsic layer. The carrier concentration in the intrinsic layer varies across the wafer in a manner that is not completely understood. Furthermore, the carrier concentration in this layer changes when changing from one manufacturer of GaN substrate to another. This effect is also not understood. At very low carrier concentrations below 10^{16} electrons per cm^3, the Si doping is compensated by other impurities (possibly carbon) and it becomes very difficult to accurately control the resulting compensated carrier density. Carrier concentrations lower than 10^{15}, while beneficial to device operation and reverse breakdown voltage, are extremely difficult to achieve for GaN and are not routinely targeted. Capacitance-voltage measurements are used to determine the carrier concentration at various positions across the wafer and are used as a method of routinely monitoring the carrier density.

The compensated carrier density directly impacts the maximum achievable reverse bias breakdown voltage. This maximum voltage is rarely achieved in practice, but with an effective junction edge termination scheme, it is possible to achieve actual reverse breakdown voltages of 90% of the theoretical maximum for a hypothetical semi-infinite diode without edges. This highlights the importance of understanding junction edge termination on a deeper level in order

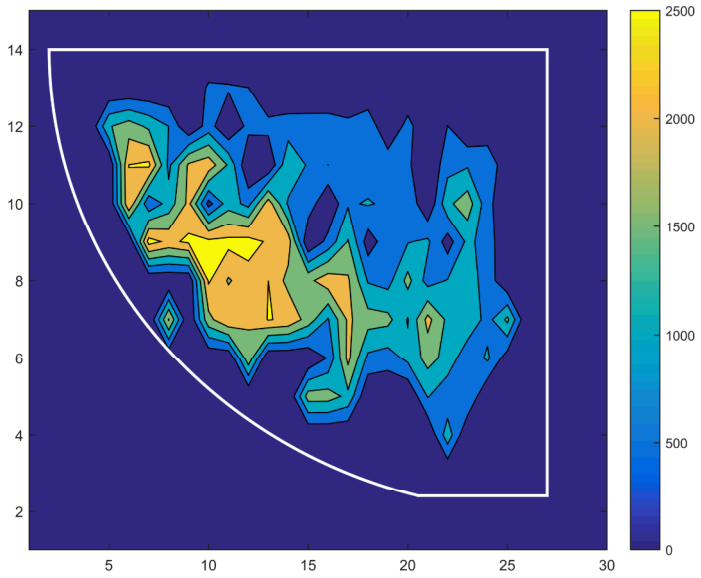

Fig. 4. Contour plot showing measured reverse bias breakdown voltage as a function of position on a quarter of a two inch wafer. The axes show units in millimeters and the colored scale is voltage in volts.

to maximize device performance.

We have developed an understanding of the junction edge termination based on a simple geometry where a thin layer of material with a lower hole concentration is left behind after implant at the edge of a GaN pin diode. Although this edge termination scheme requires careful layer thickness control, it is ultimately a simpler and more reproducible method of edge termination as it does not require a complicated ring structure with very small lithographic features.

ANTICIPATED IMPACT:

The research work conducted for this exploratory express LDRD has led to a deeper understanding of edge termination in GaN pin diodes. Edge termination in high voltage devices is extremely important for high voltage diodes. If we consider the semi-infinite case with no edge termination, the breakdown voltage is determined primarily by the carrier concentration in the intrinsic region and the thickness of the intrinsic region. Thicker intrinsic regions with lower carrier concentrations lead to higher breakdown voltages. Although this is well understood conceptually, further work needs to be done to understand the growth and measurement of thick intrinsic layers with very low carrier concentrations. For example, it is possible that the compensated carrier concentration varies as a function of depth into the 15 micron thick intrinsic region. Preliminary capacitance-voltage measurements from fully fabricated devices indicate that there may in fact be a variation in carrier concentration as a function of depth through the intrinsic layer. This will require further test and analysis to definitively measure the depth dependence of the carrier concentration and assess the impact on device performance.

The breakdown voltage in the semi-infinite case without any edges is merely a theoretical number and cannot be realized for an actual device. The edges of the device, if not properly terminated, will enable premature breakdown at much lower voltages than are possible for a theoretical device with no edge termination. Therefore, the goal of edge termination is to come up with a simple method which achieves the maximum reverse bias voltage for a real device which is hopefully 90% or better of the maximum voltage possible for an infinite device with no edges. This analysis highlights the impact of the work done on this project. We have developed a simple edge termination method that has shown reverse bias voltages as high as 2.7 kV.

This work also highlights the importance of very accurately knowing the p-GaN thickness. As a part of this work, we also attempted to measure the thickness of the p-GaN using white light interference measurements. We measured the total GaN thickness before and after the growth of a p-GaN layer. Unfortunately, these measurements were not particularly conclusive. For future work we plan to measure the p-GaN thickness for a fully fabricated device. There are several methods which can be used to measure this thickness. One method would be to perform a cut with a focused ion beam and then measure the thickness of the p-GaN in the cross-sectional cut using a SEM. However, the contrast from a thin p-GaN cap layer might not be distinguishable from the normal enhanced emission of secondary electrons from the region near the top of the sample. Another idea is to perform a capacitance measurement before the Mg in the p-GaN is activated. This would actually be a measurement before device fabrication, but could yield very useful information about the p-GaN thickness at different positions across a wafer. A third method would be to perform a capacitance-voltage measurement at low temperatures where the Mg acceptors are frozen out. This would essentially be a capacitance measurement of the

insulating Mg-doped GaN to determine the layer thickness. In any case, these measurements are a work in progress and will be the subject of future investigations.

Finally, we have determined that a capacitance measurement is a very quick and routine method of determining which devices on a wafer will have the best reverse bias voltage characteristics. Essentially a device with a high capacitance will have a higher reverse bias breakdown voltage. This is a quick and easy way to screen devices to determine the best wafers or the best regions on a particular wafer.

This work has helped us to understand GaN pin diodes in much greater detail. We now have a simple method of edge terminations for GaN pins which we understand based on comparison between experimental results and TCAD simulations. This will enable us to maximize the high voltage breakdown in our devices and to achieve much better device performance for a given intrinsic layer thickness and carrier concentration. Future proposals will focus on understanding the growth of intrinsic GaN layers with very low carrier concentrations as well as working on controlling and measuring layer thicknesses with greater accuracy. Based on these results, we expect to be able to demonstrate GaN pin diodes which can be operated at 5 kV or greater which will be useful for many future high power solid state switching applications.

CONCLUSION:

High voltage diodes are desired for many high power switching applications including several applications which are important to internal Sandia customers. GaN pin diodes have the potential to replace conventional silicon diodes for applications requiring very low size and weight, and high power. GaN diodes have several advantages including the ability to operate at high temperatures and a higher tolerance to radiation damage. We have developed a simple method of edge termination for GaN pin diodes. This method does not require complicated ring structures in order to demonstrate a high breakdown voltage. A combination of TCAD modeling and experimental measurements were used to validate our hypothesis that a very thin layer of p-type material with a lower hole concentration is critical to the edge termination in our devices. This work positions us well to demonstrate GaN pin diodes with reserve bias breakdown voltages of 5 kV or greater. If successful, these high voltage GaN pin diodes will revolutionize power conversion technology and enable novel systems with extremely low size and weight, and high power. This will in turn enable many new applications where improvements in size, weight, and power are particularly important and will usher in a new era where highly efficient power conversion can be obtained in extremely small packages.

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